

Sapta Girish Babu. N

CONTACT INFORMATION	Department of Communications Bharat Electronics Limited Bangalore, Karnataka, India	☎ : (+91) 9019918273 ✉ : girish966@gmail.com www.iitgalumni.org/sapta
CAREER OBJECTIVE	To work in a creative, challenging and competitive environment where I can strive for growth , in terms of value addition, knowledge and learning, thereby; striving to optimize a goal congruent behavior, thereby elevating self and organization into higher and profitable pinnacles.	
TECHNICAL SKILLS	<ul style="list-style-type: none">• Software: Cadence, Mentor Graphics, Xilinx ISE , Matlab, Simulink, Modelsim• Hardware Description Languages: Verilog, VHDL• DSP Processors: Working knowledge on ADSP 2189, ADSP 2191, TMS6446• Middle Level Languages: C• Scripting Languages: Working knowledge on Perl, Unix shell scripting• Operating Systems: Working Knowledge on Linux, Windows• Miscellaneous: Excellent trouble shooting and debugging skills	
PROFESSIONAL EXPERIENCE 1	Central Research Laboratory, B.E.L Bangalore	October 2009 - till date
	Project Title : Design and Development of Software Defined Radio.	
	HDL used : Verilog	FPGA's used : Xilinx Virtex 4, Spartan 6
	My contribution in the Project :	
	<ul style="list-style-type: none">• Configured peripherals such as ADC(ADS5500), DAC(DAC5687), CDCM(CDCM7005), DDS(AD9957), P-Z Filter through SPI interface and CODEC(TLV320AIC3107) through I²C interface in Virtex 4 FPGA in Verilog HDL.• Implemented FM Modem for IF of 21.4 MHz, deviation of 8 KHz in FPGA and tested Voice Communication between two radios through RF.• Simulated the Transmitter and Receiver algorithms in MATLAB for FSK Modem and MSK Modem and implemented in FPGA at a data rate of 2.304 Mbps and tested the data communication between two radios.• Realized Signal processing functions like implementation of third order CIC filter, FIR filter, IIR filter, 12 level CORDIC algorithm in FPGA.• Configured HI-6110 MIL-STD-1553 Message processor in Spartan 6 FPGA for Bus Controller mode and Remote terminal mode and tested the communication between two boards.• Presently working on TMS320DM6446 processor.	

POST GRADUATE FINAL YEAR PROJECT	<p>Indian Institute of Technology Guwahati</p> <p>Project Title : Tri State Integer Cycle Modulation</p> <p>HDL used : Verilog Softwares used : ADSP 2189, Matlab</p> <p>Boards used : Xilinx Virtex II Pro FPGA</p> <p>Abstract :</p> <p>The expansion of Tele communication services is continuing, particularly with the introduction of PCS. A large part of the telecommunications infrastructure depends on the use of Radio Frequency spectrum. With ever increasing number of applications, the radio spectrum has become a scarce commodity. Our work is concerned with the investigation of a new kind of continuous phase FSK-type modulation scheme to facilitate data transfer at a high data rate with effective utilization of bandwidth. The transmitter and the receiver structure that makes this modulation scheme suitable for wireless environment is simulated in Matlab and implemented on Virtex II Pro FPGA and ADSP 2189 Processor.</p>
PAPERS PRESENTED	<p>Presented a technical paper titled Transceiver Structure for Tri State Integer Cycle Modulation at IEEE Conference on Communications, Networking and Computing (CNC 2010) at Calicut, Kerala.</p>
PROFESSIONAL EXPERIENCE 2	<p>Qualcore Logic Limited, Hyderabad August 2006 - May 2007</p> <p>Designation : Engineer Trainee</p> <p>Got Trained on the entire ASIC flow, from Design to Verification including DFT and Synthesis. Designed a block of HDMI protocol in Verilog language using Cadence tools - NC verilog and verified using System Verilog language.</p>
EDUCATION	<p>Indian Institute of Technology, Guwahati, Assam</p> <p>M.Tech., Digital Signal Processing, 2007 - 2009 CPI: 9.48 /10 (Four semesters)</p> <p>CBIT, Osmania University, Hyderabad, Andhrapradesh</p> <p>B.E., Electronics and Communication Engineering, 2002-2006 Percent Marks: 84 % (average of all semesters)</p> <p>Sri Chaitanya, Vijayawada, Andhrapradesh</p> <p>Intermediate, Board of Intermediate Education , 2000-2002 Percent Marks: 97%</p> <p>Viswavani, Vijayawada, Andhrapradesh</p> <p>Xth, Board of Secondary Education , 1999-2000 Percent Marks: 86 %</p>
HONORS AND AWARDS	<ul style="list-style-type: none"> • Achieved National Wide Merit Scholarship Certificate from Ministry of Human Resource Development - Govt. of India • All India Rank 540 (98.2 percentile) in Graduate Aptitude Test in Engineering (GATE), 2007 in Electronics and Communication Engineering. • State level Rank 587 in Andhra Pradesh Common Entrance Test (EAMCET) for Engineering admission, 2002

POST GRADUATE **Speech Recognition**

COURSE A large data base is collected and speech recognition for digits is done.

MINI PROJECTS **Implementation of FFT algorithm on ADSP 218x processor**

FFT algorithm is implemented on ADSP 218x processor

Other Lab projects

Some blocks of the Text to Speech Synthesis system are developed and a seminar is given on the same topic.

COURSE WORK

Digital Signal Processing	Speech Processing
Digital Integrated Circuits	Analog Integrated Circuits
Statistical Signal Processing	Advanced Digital Signal Processing

PERSONAL PROFILE

Name	Sapta Girish Babu. Neelam
Fathers Name	Koteswara Rao. Neelam
Date of Birth	22-08-1985
Marital Status	Single
Nationality	Indian
Hobbies	listening to radio, playing chess
E-mail	girish966@gmail.com
Phone No	09019918273 , 0866-2586026
Languages	English, Hindi, Telugu
Temporary Address	Sapta Girish Babu, Member(Research Staff); Central Research Laboratory, B.E.L Bangalore, Karnataka - 560013

REFERENCE

Dr. Anil Mahanta,
Professor, Department of ECE, IIT Guwahati
✉ : anilm@iitg.ernet.in